when the period and width updates/changes 310 and 320 occur across the PWM cycle boundary ~~310~~ 330 in a sequence as shown in PWM cycles 340, 350, and 360.

IN THE CLAIMS

Please amend the claims as follows:

1. (Cancelled)

2. (Currently Amended) An apparatus comprising a PWM waveform generator to generate a predictable pulse width modulated (PWM) signal, on a real-time basis, based on a sequence of combinations of programmed period and width values and their associated primary period and primary width updates received from a processor,

wherein the PWM signal includes a sequence of PWM cycles, wherein each PWM cycle includes a PWN signal boundary,

wherein each of the received primary period and primary width updates can occur across or within each PWM signal boundary of a current PWM signal being generated.

3. (Previously presented) The apparatus of claim 2, wherein the PWM waveform generator comprises:

primary period and primary width storage elements, wherein the received period and width values are stored in the primary period and primary width storage elements upon receiving the primary period and primary width updates from the processor, respectively;

secondary period and secondary width storage elements coupled to the primary period and primary width storage elements, respectively, to receive the period and width values from the primary period and primary width storage elements and to store the received period and width values in the secondary period and secondary width storage elements, respectively, upon receiving a secondary storage element write control signal;

a tertiary period storage element coupled to the secondary period storage element to receive the period value from the secondary period storage element based on a tertiary period register write signal and to store the period value in the tertiary storage element;

a down-counter coupled to the secondary width storage element and the tertiary period storage element to receive the width value from the secondary width storage element upon receiving a width update counter signal, wherein the down-counter to countdown the loaded width value in each clock cycle until the down-counter reaches zero, wherein the period value is then loaded into the down-counter from the tertiary period storage element, wherein the down-counter counts down every clock cycle until it reaches zero, and wherein the down-counter generates an EXPIRE signal upon reaching the zero; and

a final output waveform generator coupled to the down-counter to receive the EXPIRE signal from the down-counter and to generate the PWM signal on a real-time basis.

4. (Previously presented) The apparatus of claim 3, wherein the PWM waveform generator further comprises:

a state machine coupled to the down-counter, final output waveform generator, wherein the state machine is to receive the EXPIRE signal from the down-counter and to generate a state signal.

5. (Original) The apparatus of claim 4, wherein in the PWM waveform generator further comprises a data bus coupled between the processor and the primary period and primary width storage elements to transmit the period and width values and their associated primary period and primary width updates from the processor to the primary period and primary width storage elements.

6. (Previously presented) The apparatus of claim 5, wherein the PWM waveform generator further comprises:

a timing controller coupled to the processor via the data bus and the down-counter to generate the secondary storage element write control signal upon receiving the primary width update from the processor, wherein the timing controller to generate the tertiary period register write signal based on the EXPIRE signal received from the down-counter and the state value received from the state machine, wherein the tertiary period register write signal is a single clock-cycle pulse at the current PWM signal boundary, wherein the final output waveform

generator to internally generate expired width and expired period signals using the EXPIRE signal along with the state value, and wherein the timing controller to further generate the width update counter signal based on the expired period signal and a period update counter signal based on the expired width signal.

7. (Previously presented) The apparatus of claim 6, wherein the PWM waveform generator further comprises:

a configuration storage element coupled to the processor via the data bus to receive a control signal upon receiving the period and width values from the processor through the data bus and to output a configuration signal, wherein the final output waveform generator generates the PWM signal or an inverse of the PWM signal based on the expired period and width signals and the configuration signal.

8. (Currently Amended) The apparatus of claim 7, wherein the PWM waveform generator further comprises:

a subtractor coupled between the primary period storage element and the secondary period storage element and further coupled to the primary width storage element, wherein the subtractor to receive the width value from the primary width storage element and the period value from the primary period storage element and to compute a secondary period value using the received period and width values, wherein the tertiary storage element is to receive the secondary period value upon receiving the tertiary period register write signal from the timing controller, and wherein the down-counter is to receive the secondary period value from the tertiary period storage element upon receiving the period update counter signal and to output the EXPIRE signal corresponding to the expired period signal.

9. (Previously presented) An apparatus for generating a (pulse width modulated) PWM waveform based on a sequence of combinations of programmed period and width values received from a processor, comprising:

a primary period storage element to store a current programmed period value upon receiving a primary period storage element write signal from the processor;

a primary width storage element to store a current programmed width value upon receiving a primary width storage element write signal from the processor;

a down-counter to generate an EXPIRE signal upon reaching a zero value;

a state machine to receive the EXPIRE signal from the down-counter and to generate a state signal;

a timing controller to receive the primary width storage element write signal from the processor and to output a secondary storage element write control signal upon receiving the primary width storage element write signal, wherein the timing controller to generate a tertiary period register write signal based on the EXPIRE and the state signals, and wherein the timing controller to further generate a width update counter signal and a period update counter signal based on the EXPIRE and the state signals;

a secondary width storage element to receive the current width value from the primary width storage element upon receiving the secondary storage element write control signal;

a subtractor to receive the current period and width values from the primary period storage element and the primary width storage element, respectively, and to output a secondary period value;

a secondary period storage element to receive the secondary period value from the subtractor upon receiving the secondary storage element write control signal;

a tertiary period register to receive the secondary period value from the secondary period storage element upon receiving the tertiary period register write signal from the timing controller, wherein the down-counter is to receive the current width value upon receiving the width update counter signal and to receive the secondary period value from the tertiary period register upon receiving the period update counter signal and to output the EXPIRE signal; and

a final output waveform generator to output a current PWM waveform based on the EXPIRE signal and the state signal.

10. (Original) The apparatus of claim 9, further comprising:

a configuration register to receive a control signal from the processor upon outputting the period and width values and to output a configuration signal, wherein the final output waveform generator to output the PWM waveform or its inverse based on the configuration signal.

11. (Previously Presented) The apparatus of claim 10, wherein the final output waveform generator to generate the PWM waveform having a width of one clock cycle and a period of two clock cycles.

12. (Previously Presented) The apparatus of claim 9, further comprising:

a DSP core; and

a bus coupled between the DSP core and the primary period register, the primary width register, and the configuration register to transmit the primary period value and the primary width value from the DSP core to the primary period register and the primary width register, respectively.

13. (Original) The apparatus of claim 9, wherein the primary period and primary width storage elements are memory-mapped registers.

14. (Previously Presented) A DSP system-on-chip (SoC) for generating a real-time distortionless PWM signal comprising:

a DSP core to receive current programmed period and width values and their associated period and width update signals from an user program;

a data bus coupled to the core;

primary period and primary width registers coupled to the data bus to store the current programmed period and width values in the primary period and primary width registers upon receiving the period and width write signals, respectively, from the DSP core via the data bus;

secondary period and secondary width registers coupled to the primary period and primary width registers, respectively, to receive the current programmed period and width values from the primary period and primary width registers upon receiving a secondary storage element write control signal;

a tertiary period register coupled to the secondary period register to store the period value at a beginning boundary of a cycle of the PWM signal;

a down-counter coupled to the secondary width register and the tertiary period register to receive the current programmed width value at the beginning boundary of the PWM signal, wherein the period value is then loaded into the down-counter from the tertiary period storage element, wherein the down-counter counts down every clock cycle until it reaches zero, and wherein the down-counter generates an EXPIRE signal upon reaching the zero; and

a final output waveform generator coupled to the down-counter to receive the EXPIRE signal and to generate the PWM signal.

15. (Original) The DSP SoC of claim 14, further comprising:

a subtractor coupled to the primary period and primary width registers and the secondary period register to receive the current programmed period and programmed width values from the primary period and primary width registers and to generate a secondary period value by subtracting the current programmed width value from the current programmed period value.

16. (Original) The DSP SoC of claim 15, further comprising:

a timing controller coupled to the data bus, the down-counter, the secondary period and secondary width registers, and the tertiary period register, to generate the secondary storage element write control signal upon receiving the width write signal from the DSP core via the data bus, wherein the timing controller to receive the secondary period value and the current programmed width value and to generate a tertiary period register write signal based on the EXPIRE signal, and wherein the timing controller to further generate a width write counter signal based on the current programmed width value and a period write counter signal based on the secondary period value.

17. (Previously Presented) The DSP SoC of claim 16, further comprising a state machine coupled to the timing controller, the down-counter, and the final output waveform generator to receive the EXPIRE signal from the down-counter and to generate a state signal, wherein the final output waveform generator to internally generate expired width and expired period signals using the EXPIRE signal and the state signal.

18. (Previously presented) The DSP SoC of claim 16, wherein the down-counter to generate the EXPIRE signal corresponding to an expired width value based on the current programmed width value upon receiving the width write counter signal from the timing controller, and wherein the down-counter to receive the secondary period value from the tertiary period register upon generating the EXPIRE signal and to again generate the EXPIRE signal based on the secondary period value upon receiving the period write counter signal.

19. (Original) The DSP SoC of claim 18, further comprising:

a configuration register coupled to the data bus and the final output waveform register to receive a control signal from the processor upon outputting the period and width values and to output a configuration signal, wherein the final output waveform generator to generate the PWM signal or an inverse of the PWM signal based on the configuration signal.

20. (Canceled)

21. (Previously presented) An audio processor comprising a system-on-chip (SoC), wherein the SoC comprises:

primary period and primary width storage elements, wherein received period and width values are stored in the primary period and primary width storage elements upon receiving the period and width updates from the audio processor, respectively;

secondary period and secondary width storage elements coupled to the primary period and primary width storage elements, respectively, to receive the primary and width values from the primary period and primary width storage elements and store in the secondary period and secondary width storage elements, respectively, upon receiving the width update;

a tertiary period storage element coupled to the secondary period storage element to receive the period value from the secondary period storage element based on a tertiary period register write signal and to store the period value in the tertiary storage element;

a down-counter coupled to the secondary width storage element and the tertiary period storage element to receive the width value from the secondary width storage element upon

receiving a width write counter signal, wherein the down-counter to generate an EXPIRE signal upon reaching a zero value; and

a final output waveform generator coupled to the down-counter to receive the EXPIRE signal from the down-counter and to generate the PWM signal on a real-time basis.

22. (Original) The audio processor of claim 21, wherein the primary period and primary width storage elements are memory mapped registers.

23. (Currently Amended) A microcontroller for generating a distortionless PWM signal on a real-time basis comprising:

means for storing a programmed period value upon receiving a primary period storage element write signal from a microcontroller core;

means for storing the programmed width value upon receiving a primary width storage element write signal from the microcontroller core;

means for counting down the period and width values and generate an expired period signal and an expired width signal;

means for receiving the primary width storage element write signal from the microcontroller core and to output a secondary storage element write control signal upon storing the width value, wherein the means ~~to receive~~ for receiving the primary width storage element write signal ~~to generate~~ generates a tertiary period register write signal based on the expired period signal , and wherein the means ~~to receive~~ for receiving the primary width storage element write signal ~~to further generate~~ further generates a width update counter signal based on the expired period signal and a period update counter signal based on the expired width signal;

means for receiving the width value upon receiving the secondary storage element write control signal;

means for receiving the period and width values and subtract the width value from the period value and to output a secondary period value;

means for receiving the secondary period value upon receiving the secondary storage element write control signal;

means for receiving the secondary period value upon receiving the tertiary period register write signal;

means for receiving the width value upon receiving the width update counter signal and to further receive the secondary period value upon receiving the period update counter signal and to output ~~an~~ the expired width signal based on received width value and ~~an~~ the expired period signal based on the secondary period value; and

means for outputting the PWM signal based on the expired period and width signals.

24. (Currently Amended) The microcontroller of claim 23, further comprising:

~~a means to receive~~ means for receiving the period and width values from the microcontroller core and to output a configuration signal, wherein the ~~final output waveform generator~~ means for outputting the PWM signal generates ~~to generate~~ the PWM signal based on the configuration signal.

25. (Canceled)

26. (Canceled)

27. (Previously Presented) A method for generating a predictable pulse width modulated (PWM) signal on a real-time basis based on a sequence of combinations of the programmed period and width values, wherein each of the received combinations of the programmed period and width write updates can occur across or within a PWM signal boundary of a current PWM signal being generated, comprising:

receiving the sequence of combinations of the programmed period and width values and their associated primary period and width write signals;

storing each of the programmed period and width values in primary period and width registers, upon receiving the primary period write and width write signals, respectively;

storing the programmed width value by obtaining the programmed width value from the primary width register into a secondary width register upon receiving a secondary storage element write control signal;

computing a secondary period value by subtracting the programmed width value from the programmed period value;

storing the secondary period value into a secondary period register upon receiving the secondary storage element write control signal;

storing the secondary period value in a tertiary period register upon receiving a tertiary period register write signal;

loading a down-counter with the programmed width value by obtaining the programmed width value from the secondary width register upon receiving the width update counter signal;

counting the loaded programmed width value each clock signal to produce an expired width signal;

loading the secondary period value into the down-counter upon producing the expired width signal and upon receiving a period update counter signal;

counting the loaded secondary period value each clock signal to produce an expired period signal; and

generating the PWM signal based on the expired period and width signals.

28. (Original) The method of claim 27, further comprising:

generating a configuration signal upon receiving a control signal; and

generating the PWM signal based on the configuration signal and the expired period and width signals.

29. (Original) The method of claim 27, wherein counting the loaded programmed width value according to width timing signal to produce the expired width signal comprises:

loading the programmed width value corresponding to the width update counter signal; and

counting down the loaded programmed width value with each clock cycle until the down-counter reaches zero and then to produce the expired width signal.

30. (Original) The method of claim 27, wherein counting the loaded secondary period value according to a period timing signal to produce the expired period signal comprises:

loading the programmed secondary period value corresponding to the period update counter signal; and

counting down the loaded secondary period value with each clock cycle until the down-counter reaches zero and then to produce the expired period signal.

31. (Original) The method of claim 27, further comprising:

generating the secondary storage element write control signal upon receiving the primary width register write signal; and

generating the tertiary period register write signal based on the expired period signal.